Amendments to the Claims

Please amend the claims as follows:

1. (Original) An integrated circuit testing method comprising:

a reading step wherein circuit data is read out by a circuit data reading unit;

a path cut step wherein a path cut point is selected from a target circuit and a state is fixed by a path cut countermeasure unit; and

an automatic test pattern generating step wherein test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target is generated by an automatic test pattern generation unit,

wherein said automatic test pattern generating step comprises:

a narrowing step wherein an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group is specified as a processing target circuit by a narrowing processing unit;

a failure exciting step wherein states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure are allocated to said failure presumption points by a failure exciting unit;

a path activating step wherein states at the sending time and the receiving time for activating a propagating path of said failure are allocated to the residual preparation FFs and sending FFs by a failure propagating state setting unit; and

a failure propagating step wherein, by an automatic test pattern generation control unit, a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds, and further,

in said path activating step, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure, and

in said failure propagating step, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

2. (Original) A method according to claim 1, wherein said don't care X is a logic value constructing the test pattern which does not exert an influence on a failure detection ratio even if it is replaced with an opposite value.

3. (Original) A method according to claim 1, wherein after said failure propagating step is finished, said method comprises:

a compaction failure exciting step wherein the don't care X in said path activating step changes to a value opposite to that of the state at the receiving time and the state of the failure excitation is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending

FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating the state for detecting the delay failure to the path between the sending FF and the receiving FF and generating the test pattern when the propagation succeeds.

4. (Original) A method according to claim 1, wherein in said failure exciting step, when a clock-off is allocated to the sending FF at the sending time, an uncontrol value (u) showing that the failure excitation is impossible for a failure value is conditional-implicated in an output of said sending FF at the receiving time, the allocation itself of said uncontrol value (u) is determined that the failure excitation is impossible, and the failure is excluded from targets of the delay failure.

5. (Original) A method according to claim 1, wherein when the failure propagation fails in said failure propagating step, among the failures which are presumed into the network from the network in which the failed failure has been presumed to a branch input of a fan-out free area, the failure in which the inverting relation is equal to that of the failed failure and a failure value is equal to a control value of a gate is extracted and excluded as an undetectable failure.

6. (Original) A method according to claim 1, wherein in said path cut step, in a gate input of driving the path cut point, a control value of a gate is given at the sending time and the receiving time and the state is fixed, or the uncontrol value of the gate is given to all gate inputs at the sending time and the receiving time and the state of said path cut point is fixed by allocating a fixed state "from 0 to 0" or "from 1 to 1".

7. (Original) A method according to claim 6, wherein said path cut step has a fixed state selecting step wherein, with respect to the fixed state "from 0 to 0" or "from 1 to 1" which is allocated to the path cut point, a failure detection impossible number is measured by said automatic test pattern generating step and the fixed state whose failure detection impossible number is small is selected.

8. (Original) A method according to claim 6, wherein said path cut step has a hazard-freeing step wherein in the case where a transfer in which a pin input position of the control value changes at the sending time and the receiving time exists among a plurality of input pins of the driver side gates for the path cut point, by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time, the hazard-free fixed state is generated for the path cut point.

9. (Original) A method according to claim 1, wherein in said narrowing step, as a preparation of said failure exciting step, a narrowing range is marked by back traces of two stages from the failure presumption point to the sending FF group via the receiving FF and from the sending FF group to the preparation FF group, and if both states at the sending time and the receiving time of the network are not the don't care X, the back trace after the network is stopped.

10. (Original) A method according to claim 9, wherein in said automatic test pattern generating step, if the detection of the delay failure fails with respect to either the leading delay failure or the trailing delay failure of the same network, the unmarking of the narrowing range which has been marked by the back trace in said

narrowing step is not performed but the mark is used as it is, and the test pattern generation is executed by using the other undetected delay failure as a target.

11. (Currently Amended) A ~~program for allowing a computer to execute~~ computer-readable storage medium storing a computer-readable program for executing a method of testing an integrated circuit, said method comprising the steps of:

a reading step wherein circuit data is read out;

a path cut step wherein a path cut point is selected from a target circuit and a state is fixed by a path cut countermeasure unit; and

an automatic test pattern generating step wherein test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target is generated,

wherein said automatic test pattern generating step allows the computer to execute:

a narrowing step wherein an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group is specified as a processing target circuit;

a failure exciting step wherein states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure are allocated to said failure presumption points;

a path activating step wherein states at the sending time and the receiving time

for activating a propagating path of said failure are allocated to the residual preparation FFs and sending FFs; and

a failure propagating step wherein a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds,

and further, in said path activating step, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure, and

in said failure propagating step, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

12. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 11, wherein said don't care X is a logic value constructing the test pattern which does not exert an influence on a failure detection ratio even if it is replaced with an opposite value.

13. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 11, wherein after said failure propagating step is finished, said program allows the computer to execute:

a compaction failure exciting step wherein the don't care X in said path activating step changes to a value opposite to that of the state at the receiving time and the state

of the failure excitation is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is captured, thereby propagating the state for detecting the delay failure to the path between the sending FF and the receiving FF and generating the test pattern when the propagation succeeds.

14. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 11, wherein in said failure exciting step, when a clock-off is allocated to the sending FF at the sending time, an uncontrol value showing that the failure excitation is impossible for a failure value is conditional-implicated in an output of said sending FF at the receiving time, an allocation itself of said uncontrol value is determined that the failure excitation is impossible, and the failure is excluded from targets of the delay failure.

15. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 11, wherein when the failure propagation fails in said failure propagating step, among the failures which are presumed into the network from the network in which the failed failure has been presumed to a branch input of a fan-out free area, the failure in which the inverting relation is equal to that of the failed failure and a failure value is equal to a control value of a gate is extracted and excluded as an undetectable failure.

16. (Currently Amended) ~~A program~~ The computer-readable storage medium

according to claim 11, wherein in said path cut step, in a gate input of driving the path cut point, a control value of a gate is given at the sending time and the receiving time and the state is fixed, or the uncontrol value of the gate is given to all gate inputs at the sending time and the receiving time and the state of said path cut point is fixed by allocating a fixed state "from 0 to 0" or "from 1 to 1".

17. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 16, wherein said path cut step has a fixed state selecting step wherein, with respect to the fixed state "from 0 to 0" or "from 1 to 1" which is allocated to the path cut point, a failure detection impossible number is measured by said automatic test pattern generating step and the fixed state whose failure detection impossible number is small is selected.

18. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 16, wherein said path cut step has a hazard-freeing step wherein in the case where a transfer in which a pin input position of the control value changes at the sending time and the receiving time exists among a plurality of input pins of the driver side gates for the path cut point, by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time, the hazard-free fixed state is generated for the path cut point.

19. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 11, wherein in said narrowing step, as a preparation of said failure exciting step, a narrowing range is marked by back traces of two stages from the failure presumption point to the sending FF group via the receiving FF and from the sending

FF group to the preparation FF group, and if both states at the sending time and the receiving time of the network are not the don't care X, the back trace after the network is stopped.

20. (Currently Amended) ~~A program~~ The computer-readable storage medium according to claim 19, wherein in said automatic test pattern generating step, if the detection of the delay failure fails with respect to either the leading delay failure or the trailing delay failure of the same network, unmarking of the narrowing range which has been marked by the back trace in said narrowing step is not performed but the mark is used as it is, and the test pattern generation is executed by using the other undetected delay failure as a target.

21. (Currently Amended) A ~~computer readable storing medium program for allowing a computer to execute:~~ system for testing integrated circuits, comprising:

a reading ~~step wherein circuit data is read out~~ means for reading out circuit data;

a path cut ~~step wherein a path cut point is selected from a targeted circuit and a state is fixed~~ means for selecting a path cut point from a target circuit and for fixing a state by a path cut countermeasure unit; and

an automatic test pattern generating ~~step wherein~~ means for generating test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target ~~is generated;~~

~~wherein said automatic test pattern generating step allows the computer to execute;~~

a narrowing ~~step wherein an area including~~ means for specifying a processing

target circuit where the processing target circuit includes a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group ~~is specified as a processing target circuit~~;

a failure exciting ~~step wherein~~ means for allocating states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure ~~are allocated~~ to said failure presumption points;

a path activating ~~step wherein~~ means for allocating states at the sending time and the receiving time for activating a propagating path of said failure ~~are allocated~~ to the residual preparation FFs and sending FFs; and

a failure propagating ~~step wherein~~ means for sending a system clock ~~is supplied~~ as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, and for supplying the system clock ~~is supplied~~ as a receiving clock to said receiving FF, and the network change is captured, thereby propagating a state for detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds,

and further, in said path activating ~~step~~ means, an allocation of a don't care X is permitted as a state for activating the propagating path of the failure, and

in said failure propagating ~~step~~ means, after the change in network, the state is transferred from the don't care X to an uncontrol value, thereby activating the propagating path of the failure.

22. (Original) An integrated circuit testing apparatus comprising:

a circuit data reading unit which reads out circuit data;

a path cut countermeasure unit which selects a path cut point from a target circuit and fixes a state; and

an automatic test pattern generation unit which generates test data to detect a delay failure with respect to the circuit whose path cut has been finished as a target,

wherein said automatic test pattern generation unit comprises:

a narrowing unit which specifies an area including a sending FF group corresponding to failure presumption points, a receiving FF, and further, a preparation FF group that is one-stage precedent to said sending FF group as a processing target circuit;

a failure exciting unit which allocates states of failure excitation at sending time and receiving time which have an inverting relation such that the state changes from 0 to 1 in a leading failure and changes from 1 to 0 in a trailing failure to said failure presumption points;

a failure propagating state setting unit which allocates states at the sending time and the receiving time for activating a propagating path of said failure to the residual preparation FFs and sending FFs; and

an automatic test pattern generation control unit which supplies a system clock as a sending clock to the sending FF, gives a change to a network from the sending FF and propagates the change, supplies the system clock as a receiving clock to said receiving FF, and captures the network change, thereby propagating a state for

detecting the delay failure to a path between the sending FF and the receiving FF and generating a test pattern when the propagation succeeds,

and further, said failure propagating state setting unit permits an allocation of a don't care X as a state for activating the propagating path of the failure, and

said automatic test pattern generation control unit transfers the state from the don't care X to an uncontrol value after the change in network, thereby activating the propagating path of the failure.

23. (Currently Amended) A ~~program for allowing a computer to execute~~ system for testing integrated circuits, said system comprising:

a first allocating means for allocating ~~a failure exciting step wherein~~ failure excitation states ~~showing~~ of circuit operating modes ~~of failure excitation at a sending time and a receiving time are allocated~~ to failure presumption points of a processing target circuit including a sending FF group, a receiving FF group, and further, a preparation FF group that is one-stage precedent to said sending FF group;

a second allocating means for allocating ~~a path activating step wherein~~ a state showing a circuit operating mode for activating a propagating path of [[said]] a failure at [[the]] a sending time and [[the]] a receiving time ~~is allocated~~ to the residual preparation FFs and sending FFs; and

a failure propagating ~~step wherein~~ means for supplying a system clock ~~is supplied~~ as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, and for supplying the system clock ~~is supplied~~ as a receiving clock to said receiving FF, and the network change is grasped, thereby

propagating the state showing the circuit operating mode for detecting the delay failure to a path between the sending FF and the receiving FF[[, and]];

a generating means for generating ~~when the propagation of the state showing the circuit operating mode for detecting said delay failure is successful,~~ a test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values ~~is generated~~ when a propagation of a state showing the circuit operating mode for detecting said delay failure is successful,

wherein, ~~further, as said path activating step,~~ when the state showing the circuit operating mode for activating the propagating path of the failure after said network change is a state which is shifted to an uncontrol value from a don't care value X,

the propagating path of the failure is activated by permitting said don't care value X.

24. (Previously Presented) ~~A program~~ The system according to claim 23, ~~wherein after said failure propagating step is finished, said program further allows the computer to execute~~ further comprising:

a compaction failure exciting ~~step wherein~~ means for allocating said state in which the don't care value X ~~in said path activating unit~~ is changed to a value opposite to that of the state showing the circuit operating mode at the receiving time ~~is allocated~~; and

a compaction failure propagating ~~step wherein~~ means for supplying the system clock is ~~supplied~~ as a sending clock to said sending FF, the change is given to the

network from the sending FF and propagated, and for supplying the system clock ~~is supplied~~ as a receiving clock to said receiving FF, and the network change is grasped, ~~thereby~~ and for propagating the state showing the circuit operating mode for detecting the delay failure in the path between the sending FF and the receiving FF, and

wherein the generating means generates ~~when the propagation of said state is successful,~~ a test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values ~~is generated~~.

25. (Currently Amended) A ~~program for allowing a computer to execute a step wherein~~ system for testing integrated circuits, said system comprising:

~~when~~ an allocating means for allocating a state showing a circuit operating mode of failure excitation ~~is allocated~~ to failure presumption points of a circuit for generating a test pattern for detecting a delay failure[[,]];

an implicating means for conditionally implicating ~~if a clock-off has been allocated to a sending FF at a sending time,~~ an ~~uncontrol~~ uncontrolled value (u) showing that the failure excitation is impossible ~~is conditional implicated~~ in a failure value corresponding to an output of said sending FF at a receiving time when a clock-off has been allocated to a sending FF at a sending time, and

an exclusion means for excluding said failure presumption points from targets of the delay failure when said uncontrol value (u) has been allocated to said failure presumption points, and when it is determined that the failure excitation is impossible~~, and said failure presumption points are excluded from targets of the delay failure~~.

26. (Currently Amended) A ~~program for allowing a computer to execute a step wherein~~ system for testing integrated circuits, said system comprising:

a detecting means for detecting a failure when failure propagation of a circuit to generate a test pattern for detecting a delay failure ~~fails,~~;

a presumption means for presuming ~~among the failures which are presumed on a network from failure presumption points, on the network, where the failure which failed in~~ said failure propagation ~~has been presumed~~ to a branch input in a fan-out free area where a circuit having a branch output does not exist[[,]];

an extracting means for extracting a ~~the failure in which an inverting relation of a failure value is equal to that of said failed failure and the~~ failure value that is equal to a control value of a gate ~~is extracted~~ where the failure in which an inverting relation of a failure value is equal to that of said failed failure[[,]]; and

an excluding means for ~~thereby~~ excluding the failure presumed on said network as an undetectable failure.

27. (Currently Amended) A ~~program for allowing a computer to execute a step wherein~~ system for testing integrated circuits, said system comprising:

a generating means for generating a test pattern for detecting a delay failure in a gate input for driving a path cut point of a circuit ~~to generate a test pattern for detecting a delay failure,~~;

a fixing means for fixing a state showing a circuit operating mode by giving control values of a gate at a sending time and a receiving time~~, a state showing a circuit~~

~~operating mode is fixed~~, or by giving an uncontrol value of the gate to all gate inputs at the sending time and the receiving time[[,]]; and

an allocating means for allocating a fixed state having a change "from 0 to 0" or "from 1 to 1" ~~is allocated~~ as said state showing the circuit operating mode at said path cut point, thereby fixing said state.

28. (Currently Amended) A ~~program~~ system according to claim 27, ~~wherein said program further allows the computer to execute a step wherein~~ further comprising:

a generating means for generating a hazard-free fixed state for said path cut point in the case where a transfer accompanied with a change in pin input position of the control value exists among a plurality of input pins of the driver side gates to drive said path cut point between the sending time and the receiving time, and

by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time[[,]]

~~a hazard-free fixed state is generated for said path cut point~~.

29. (Currently Amended) A ~~program for allowing a computer to execute a narrowing step wherein~~ system for testing integrated circuits, said system comprising:

a marking means for marking a narrowing range ~~is marked~~ by back traces of two stages from a failure presumption point of a circuit to generate a test pattern for detecting a delay failure to a sending FF group via a receiving FF group and from the sending FF group to a preparation FF group[[,]]; and

a stopping means for stopping the execution of the back trace if both states showing a circuit operating mode at the sending time and the receiving time of a network are not a don't care value X~~, execution of the back trace after the network is stopped~~.

30. (Currently Amended) A ~~program~~ system according to claim 29, wherein

if the detection of the delay failure fails with respect to either a leading delay failure or a trailing delay failure of the same network,

the mark of the narrowing range performed in the back trace of said narrowing is not erased but said mark is used as it is,

thereby executing the test pattern generation by using the other delay failure, as a target, whose delay failure is not detected.

31. (Previously Presented) A computer-readable storing medium which stores a program, wherein said program stores the following steps which are executed by a computer:

a failure exciting step wherein states showing circuit operating modes of failure excitation at a sending time and a receiving time are allocated to

failure presumption points of a processing target circuit including a sending FF group, a receiving FF group, and further, a preparation FF group that is one-stage precedent to said sending FF group;

a path activating step wherein a state showing a circuit operating mode for activating a propagating path of said failure at the sending time and the receiving time is allocated to the residual preparation FFs and sending FFs; and

a failure propagating step wherein a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting the delay failure to a path between the sending FF and the receiving FF, and

when the propagation of the state showing the circuit operating mode for detecting said delay failure is successful, a test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated, and

further, as said path activating step, when the state showing the circuit operating mode for activating the propagating path of the failure after said network change is a state which is shifted to an uncontrol value from a don't care value X,

the propagating path of the failure is activated by permitting said don't care value X.

32. (Previously Presented) A medium according to claim 31, wherein after said failure propagating step is finished, said program further stores:

a compaction failure exciting step wherein said state in which the don't care value X in said path activating step is changed to a value opposite to that of the state showing the circuit operating mode at the receiving time is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting the delay failure in the path between the sending FF and the receiving FF, and

when the propagation of said state is successful, the test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated.

33. (Previously Presented) A computer-readable storing medium which stores a program, wherein said program stores the following steps which are executed by a computer:

when a state showing a circuit operating mode of failure excitation is allocated to failure presumption points of a circuit for generating a test pattern for detecting a delay failure,

if a clock-off has been allocated to a sending FF at a sending time, an uncontrol value (u) showing that the failure excitation is impossible is conditional-implicated in a failure value corresponding to an output of said sending FF at a receiving time, and

when said uncontrol value (u) has been allocated to said failure presumption points, it is determined that the failure excitation is impossible, and said failure presumption points are excluded from targets of the delay failure.

34. (Previously Presented) A computer-readable storing medium which stores a program, wherein said program stores the following steps which are executed by a computer:

when failure propagation of a circuit to generate a test pattern for detecting a delay failure fails,

among the failures which are presumed on a network from failure presumption points, on the network, where the failure which failed in said failure propagation has been presumed to a branch input in a fan-out free area where a circuit having a branch output does not exist,

the failure in which an inverting relation of a failure value is equal to that of said failed failure and the failure value is equal to a control value of a gate is extracted,

thereby excluding the failure presumed on said network as an undetectable failure.

35. (Currently Amended) A computer-readable storing medium which stores a program, wherein said program stores the following steps which are executed by a computer:

generating a test pattern for detecting a delay failure in a gate input for driving a path cut point of a circuit ~~to generate a test pattern for detecting a delay failure,~~;

fixing a state showing a circuit operating mode by giving control values of a gate at a sending time and a receiving time~~, a state showing a circuit operating mode is fixed~~, or by giving an ~~uncontrol~~ uncontrolled value of the gate to all gate inputs at the sending time and the receiving time[[,]]; and

allocating a fixed state having a change "from 0 to 0" or "from 1 to 1" ~~is allocated~~ as said state showing the circuit operating mode at said path cut point, thereby fixing said state.

36. (Currently Amended) A medium according to claim 35, wherein said program further stores a step wherein:

generating a hazard-free fixed state for said path cut point in the case where a transfer accompanied with a change in pin input position of the control value exists among a plurality of input pins of the driver side gates to drive said path cut point between the sending time and the receiving time, and

by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time[[,]]

~~a hazard-free fixed state is generated for said path cut point~~.

37. (Previously Presented) A computer-readable storing medium which stores a program, wherein said program stores the following narrowing step which is executed by a computer:

a narrowing range is marked by back traces of two stages from a failure presumption point of a circuit to generate a test pattern for detecting a delay failure to a

sending FF group via a receiving FF group and from the sending FF group to a preparation FF group, and

if both states showing a circuit operating mode at the sending time and the receiving time of a network are not a don't care value X, execution of the back trace after the network is stopped.

38. (Previously Presented) A medium according to claim 37, wherein said program further stores a step wherein:

if the detection of the delay failure fails with respect to either a leading delay failure or a trailing delay failure of the same network,

the mark of the narrowing range performed in the back trace of said narrowing is not erased but said mark is used as it is,

thereby executing the test pattern generation by using the other delay failure, as a target, whose delay failure is not detected.

39. (Previously Presented) A pattern forming method of forming a test pattern for detecting a delay failure of a circuit, comprising:

a failure exciting step wherein states showing circuit operating modes of failure excitation at a sending time and a receiving time are allocated to

failure presumption points of a processing target circuit including a sending FF group, a receiving FF group, and further, a preparation FF group that is one-stage precedent to said sending FF group;

a path activating step wherein a state showing a circuit operating mode for activating a propagating path of said failure at the sending time and the receiving time is allocated to the residual preparation FFs and sending FFs; and

a failure propagating step wherein a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting a delay failure to a path between the sending FF and the receiving FF, and

when the propagation of the state showing the circuit operating mode for detecting said delay failure is successful, a test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated,

wherein, further, as said path activating step, when the state showing the circuit operating mode for activating the propagating path of the failure after said network change is a state which is shifted to an uncontrol value from a don't care value X,

the propagating path of the failure is activated by permitting said don't care value X.

40. (Previously Presented) A method according to claim 39, wherein after said failure propagating step is finished, said method further comprises:

a compaction failure exciting step wherein said state in which the don't care value X in said path activating step is changed to a value opposite to that of the state showing the circuit operating mode at the receiving time is allocated; and

a compaction failure propagating step wherein the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting the delay failure in the path between the sending FF and the receiving FF, and

when the propagation of said state is successful, the test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated.

41. (Previously Presented) A pattern forming method comprising a step wherein:

when a state showing a circuit operating mode of failure excitation is allocated to failure presumption points of a circuit for generating a test pattern for detecting a delay failure,

if a clock-off has been allocated to a sending FF at a sending time, an uncontrol value (u) showing that the failure excitation is impossible is conditional-implicated in a failure value corresponding to an output of said sending FF at a receiving time, and

when said uncontrol value (u) has been allocated to said failure presumption points, it is determined that the failure excitation is impossible, and said failure presumption points are excluded from targets of the delay failure.

42. (Previously Presented) A pattern forming method comprising a step wherein:

when failure propagation of a circuit to generate a test pattern for detecting a delay failure fails,

among the failures which are presumed on a network from failure presumption points, on the network, where the failure which failed in said failure propagation has been presumed to a branch input in a fan-out free area where a circuit having a branch output does not exist,

the failure in which an inverting relation of a failure value is equal to that of said failed failure and the failure value is equal to a control value of a gate is extracted,

thereby excluding the failure presumed on said network as an undetectable failure.

43. (Currently Amended) A pattern forming method comprising a step wherein:

generating a test pattern for detecting a delay failure in a gate input for driving a path cut point of a circuit ~~to generate a test pattern for detecting a delay failure,~~;

fixing a state showing a circuit operating mode by giving control values of a gate at a sending time and a receiving time~~, a state showing a circuit operating mode is fixed~~,

or by giving an ~~uncontrol~~ uncontrolled value of the gate to all gate inputs at the sending time and the receiving time[[,]]; and

allocating a fixed state having a change "from 0 to 0" or "from 1 to 1" ~~is allocated~~ as said state showing the circuit operating mode at said path cut point, thereby fixing said state.

44. (Currently Amended) A method according to claim 43, further comprising a step wherein:

generating a hazard-free fixed state for said path cut point in the case where a transfer accompanied with a change in pin input position of the control value exists among a plurality of input pins of the driver side gates to drive said path cut point between the sending time and the receiving time, and

by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time[[,]]

~~a hazard-free fixed state is generated for said path cut point~~.

45. (Previously Presented) A pattern forming method comprising a narrowing step wherein:

a narrowing range is marked by back traces of two stages from a failure presumption point of a circuit to generate a test pattern for detecting a delay failure to a sending FF group via a receiving FF group and from the sending FF group to a preparation FF group, and

if both states showing a circuit operating mode at the sending time and the receiving time of a network are not a don't care value X, execution of the back trace after the network is stopped.

46. (Previously Presented) A method according to claim 45, wherein

if the detection of the delay failure fails with respect to either a leading delay failure or a trailing delay failure of the same network,

the mark of the narrowing range performed in the back trace of said narrowing is not erased but said mark is used as it is,

thereby generating the test pattern by using the other delay failure, as a target, whose delay failure is not detected.

47. (Previously Presented) A pattern forming apparatus for forming a test pattern for detecting a delay failure of a circuit, comprising:

a failure exciting unit which allocates states showing circuit operating modes of failure excitation at a sending time and a receiving time to

failure presumption points of a processing target circuit including a sending FF group, a receiving FF group, and further, a preparation FF group that is one-stage precedent to said sending FF group;

a path activating unit which allocates a state showing a circuit operating mode for activating a propagating path of said failure at the sending time and the receiving time to the residual preparation FFs and sending FFs; and

a failure propagating unit constructed in such a manner that a system clock is supplied as a sending clock to said sending FF, a change is given to a network from the

sending FF and propagated, the system clock is supplied as a receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting the delay failure to a path between the sending FF and the receiving FF, and

when the propagation of the state showing the circuit operating mode for detecting said delay failure is successful, a test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated,

wherein, further, when the state showing the circuit operating mode for activating the propagating path of the failure after said network change is a state which is shifted to an uncontrol value from a don't care value X,

said path activating unit activates the propagating path of the failure by permitting said don't care value X.

48. (Previously Presented) An apparatus according to claim 47, wherein after the process in said failure propagating unit is finished, said apparatus further comprises:

a compaction failure exciting unit which allocates said state in which the don't care value X in said path activating unit is changed to a value opposite to that of the state showing the circuit operating mode at the receiving time; and

a compaction failure propagating unit constructed in such a manner that the system clock is supplied as a sending clock to said sending FF, the change is given to the network from the sending FF and propagated, the system clock is supplied as a

receiving clock to said receiving FF, and the network change is grasped, thereby propagating the state showing the circuit operating mode for detecting the delay failure in the path between the sending FF and the receiving FF, and

when the propagation of said state is successful, the test pattern constructed by a set of input values to said sending FF group and output values of said receiving FF group as expectation values against said input values is generated.

49. (Previously Presented) A pattern forming apparatus for forming a test pattern for detecting a delay failure of a circuit, comprising:

a failure exciting unit constructed in such a manner that

when a state showing a circuit operating mode of failure excitation is allocated to failure presumption points of a circuit for generating the test pattern for detecting a delay failure,

if a clock-off has been allocated to a sending FF at a sending time, an uncontrol value (u) showing that the failure excitation is impossible is conditional-implicated in a failure value corresponding to an output of said sending FF at a receiving time, and

when said uncontrol value (u) has been allocated to said failure presumption points, it is determined that the failure excitation is impossible, and said failure presumption points are excluded from targets of the delay failure.

50. (Previously Presented) A pattern forming apparatus for forming a test pattern for detecting a delay failure of a circuit, comprising:

a failure propagating unit constructed in such a manner that

when failure propagation of a circuit to generate the test pattern for detecting a delay failure fails,

among the failures which are presumed on a network from failure presumption points, on the network, where the failure which failed in said failure propagation has been presumed to a branch input in a fan-out free area where a circuit having a branch output does not exist,

the failure in which an inverting relation of a failure value is equal to that of said failed failure and the failure value is equal to a control value of a gate is extracted,

thereby excluding the failure presumed on said network as an undetectable failure.

51. (Currently Amended) A pattern forming apparatus for forming a test pattern for detecting a delay failure of a circuit, comprising:

~~a path cut processing unit constructed in such a manner that~~

a generating means for generating a test pattern for detecting a delay failure in a gate input for driving a path cut point of a circuit ~~to generate a test pattern for detecting a delay failure,~~;

a fixing means for fixing a state showing a circuit operating mode by giving control values of a gate at a sending time and a receiving time~~, a state showing a circuit operating mode is fixed~~, or by giving an ~~uncontrol~~ uncontrolled value of the gate to all gate inputs at the sending time and the receiving time[[,]]; and

an allocating means for allocating a fixed state having a change "from 0 to 0" or "from 1 to 1" ~~is allocated~~ as said state showing the circuit operating mode at said path cut point, thereby fixing said state.

52. (Currently amended) An apparatus according to claim 51, further comprising ~~a fixed state generating unit constructed in such a manner that~~:

a generating means for generating a hazard-free fixed state for said path cut point in the case where a transfer accompanied with a change in pin input position of the control value exists among a plurality of input pins of the driver side gates to drive said path cut point between the sending time and the receiving time, and

by adding and allocating the control value at the sending time to at least one input pin to which the control value is given at the receiving time[[,]]

~~a hazard-free fixed state is generated for said path cut point~~.

53. (Previously Presented) A pattern forming apparatus for forming a test pattern for detecting a delay failure of a circuit, comprising:

a narrowing processing unit constructed in such a manner that

a narrowing range is marked by back traces of two stages from a failure presumption point of a circuit to generate a test pattern for detecting a delay failure to a sending FF group via a receiving FF group and from the sending FF group to a preparation FF group, and

if both states showing a circuit operating mode at the sending time and the receiving time of a network are not a don't care value X, execution of the back trace after the network is stopped.

54. (Previously Presented) An apparatus according to claim 53, further comprising a pattern generating unit constructed in such a manner that

if the detection of the delay failure fails with respect to either a leading delay failure or a trailing delay failure of the same network,

the mark of the narrowing range performed in the back trace of said narrowing is not erased but said mark is used as it is,

thereby executing the test pattern generation by using the other delay failure, as a target, whose delay failure is not detected.